MAIL STOP APPEAL BRIEF-PATENTS
PATENT
8008-1052

IN THE U. S. PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of	Appeal No.
Yasutaka NAKASHIBA	Conf. 2273
Application No. 10/812,282	Group 2815
Filed March 30, 2004	Examiner J. Jackson, Jr.

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

APPEAL BRIEF

MAY IT PLEASE YOUR HONORS:

1. Real Party in Interest

The real party in interest in this appeal is the current assignee, Renesas Electronics Corporation of Kawasaki, Japan.

2. Related Appeals and Interferences

None.

3. Status of Claims

Claims 23-50 were rejected and are the subject of the present appeal. Claims 1-22 have been canceled.

4. Status of Amendments

No amendments were filed following the Final rejection of

October 14, 2010.

5. Summary of Claimed Subject Matter

Claims 23 and 36 are the independent claims. The dependent claims are not being argued separately.

Claim 23

In summary, claim 23 defines a semiconductor integrated circuit device that includes a MOS varactor film (second insulating film) that is thinner than the thinnest of MOS transistor films (first insulating films), where the MOS transistor films have a plurality of different thicknesses. Thus, the second insulating film is thinner than all the first insulating films.

More specifically, claim 23 includes:

a first conductivity type substrate (Figures 3A-C, elements PSub; page 11, last line, through page 12, line 10),

MOS transistors (Figures 3A-B, elements 1, 2; page 11, last line, through page 12, line 10) disposed in the substrate and including first insulating films (Figures 3A-B, elements 4; page 2, lines 4-7, and page 3, lines 3-6, and

an MOS type varactor element (Figure 3C, element 3; page 11, last line, through page 12, line 10) disposed in the substrate and including a second insulating film (Figure 3C,

element 14; page 12, line 22, through page 13, line 6), a conductive electrode (Figure 3C, element 5; page 13, lines 7-12) and a second conductivity type well (Figure 3C, element NW2; page 12, lines 11-15),

where the second insulating film, conductive electrode and second conductivity type well form a variable capacitor (page 11, line 20),

where the first insulating films have a plurality of different thicknesses (page 18, lines 23-27),

where a thickness of the second insulating film is thinner than that of the thinnest insulating film among the first insulating films of the MOS transistors (page 16, lines 12-16; page 18, line 27, through page 19, line 1), and

where first and second diffusion layers (Figure 3C, elements N4, N5; page 4, lines 19-26) are provided at both sides of the conductive electrode, and the first and second diffusion layers are connected to a common terminal through first and second wiring line (Figure 3C, element Vb and associated wiring; page 5, lines 5-6) respectively.

Claim 36

In summary, claim 36 defines a semiconductor integrated circuit device that includes a MOS varactor film (second insulating film) that is thinner than the MOS transistor films

(first insulating films), where the MOS transistor films all have the same thickness. Thus, the second insulating film is thinner than all the first insulating films.

More specifically, claim 36 includes:

a first conductivity type substrate (Figures 3A-C, elements PSub; page 11, last line, through page 12, line 10),

MOS transistors (Figures 3A-B, elements 1, 2; page 11, last line, through page 12, line 10) disposed in the substrate and including first insulating films (Figures 3A-B, elements 4; page 2, lines 4-7, and page 3, lines 3-6), and

an MOS type varactor element (Figure 3C, element 3; page 11, last line, through page 12, line 10) disposed in the substrate and including a second insulating film (Figure 3C, element 14; page 12, line 22, through page 13, line 6), a conductive electrode (Figure 3C, element 5; page 13, lines 7-12) and a second conductivity type well (Figure 3C, element NW2; page 12, lines 11-15),

where the second insulating film, conductive electrode and second conductivity type well form a variable capacitor (page 11, line 20),

where the first insulating films all have a same thickness (page 18, lines 20-22),

where a thickness of the second insulating film is thinner

than that of the same thickness of the first insulating films of the MOS transistors (page 16, lines 12-16; page 12, line 24, through page 13, line 6), and

where first and second diffusion layers (Figure 3C, elements N4, N5; page 4, lines 19-26) are provided at both sides of the conductive electrode, and the first and second diffusion layers are connected to a common terminal through first and second wiring line (Figure 3C, element Vb and associated wiring; page 5, lines 5-6) respectively.

6. Grounds of Rejection to be Reviewed on Appeal

Whether claims 23-50 are unpatentable under 35 U.S.C. 103(a) over KUDO et al. 6,853,037 in view of O 7,088,964, the admitted prior art (APA), and COMPTON et al. 6,462,929.

7. Argument

Rejection under 35 U.S.C. 103(a) over KUDO et al., O, the APA, and COMPTON et al.

Claim 23

Claim 23 provides, among other features, that the MOS varactor film (the second insulating film) is thinner than the thinnest of the MOS transistor films (the first insulating films), where the MOS transistor films have a plurality of

different thicknesses. Thus, the second insulating film is thinner than all the first insulating films. The references do not disclose this.

KUDO et al. disclose a semiconductor device with a plurality of MOS transistors having different gate insulating film thicknesses. The film thickness of the n-channel high-voltage transistor is greater than the film thickness of the p-channel high voltage transistor, which is greater than the film thickness of the low-voltage transistor (Abstract). KUDO et al. do not disclose a film thickness of a varactor.

O discloses that CMOS varactors are generally formed using design rules for logic devices and that logic devices are generally significantly smaller than I/O devices and use a thinner gate oxide (column 11, lines 17-21). That is, the film thickness of the I/O transistor is thicker than that of the film thickness of a logic transistor, and the film thickness of the varactor is equal to that of the logic transistor.

The APA acknowledges that logic devices and I/O devices are generally formed on the same chip.

Thus, KUDO et al. dislose only the film thicknesses of the transistors, and O discloses that the logic transistor has a film thickness equal to that of the varactor. Combining the references does not suggest to the artisan that the film

thicknesses of all the MOS transistors are each to be greater than that of the varactor.

That is, the combination of these three references disclose that in a chip with logic devices and I/O devices, the thinnest gate insulating films among the MOS transistors is to be found in the logic devices. The combination merely discloses that the gate insulating film of the varactors element is the same thickness as that of a gate insulating film of the thinnest MOS transistor on the chip. There is nothing in the combination that discloses that the thickness of the second gate insulating film in the varactor element is thinner than the thinnest gate insulating film among the first gate insulating films of the MOS transistors with different thicknesses.

The Examiner relies on COMPTON et al. for the suggestion to modify the second gate insulating film so that it is thinner than the first gate insulating films.

Figure 11 of COMPTON et al. is reproduced below; this figure shows a capacitor structure.

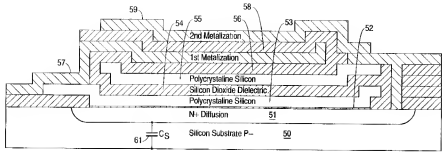

FIG. 11

This structure includes:

a p-substrate 50,

an N+ buried layer 51,

a tunnel oxide silicon oxide layer 52 less than about 100 Angstroms thick and preferably 80 Angstroms thick,

a first polysilicon layer 53 about 300 Angstroms thick,

a second silicon dioxide layer 54 about 300 Angstroms thick,

a second polysilicon layer 55,

a third silicon dioxide layer 56 several hundred Angstroms thick,

a first metallization layer 57,

a fourth silicon dioxide layer 58 several hundred Angstroms thick, and

a second metallization layer 59.

Figure 11 shows a fixed capacitor (a capacitor having a

constant capacitance regardless of voltage) that is used in charge pump circuits such as shown in Figures 9 and 10. COMPTON et al. disclose that conventional fixed capacitors have large areas and large parasitic capacitances (paragraphs 0076-77). To resolve this problem, COMPTON discloses a fixed capacitor that is formed with a tunnel oxide layer 52 that is 80 Angstroms thick, and that is used in EEPROMs.

The reference further discloses that a capacitance per unit area of a fixed capacitor formed by first polysilicon layer 53, tunnel oxide layer 52, and N+ diffusion layer 51 is 3 $fF/\mu m^2$, that a capacitance per unit area of other portions (e.g., oxide layers 54, 56) is 1 $fF/\mu m^2$, and that a total capacitance per unit area 4 $fF/\mu m^2$ (paragraphs 0081-82).

COMPTON et al. further disclose that the capacitor has a low parasitic capacitance. In the device of Figure 11, the N+ diffusion layer 51 and p-substrate 50 have a variable capacitance depending on an electric potential of the p-substrate 50 (PN junction varactor capacitance: capacitance that varies depending on the voltage), which is the parasitic capacitance. However, a capacitance per unit area between the N+ diffusion layer 51 and the p-substrate 50 (at 61 in Figure 11) is 0.08 $fF/\mu m^2$, which does not have any significant effect (paragraph 0083).

According to COMPTON et al., the capacitor structure disclosed therein is to be used in charge pump circuits. If the capacitor were a variable capacitor instead of fixed capacitor, the problem would arise that operation of the charge pump circuit using a variable capacitor would be unstable because the capacitance would vary depending on the voltage applied to a terminal of the capacitor. Thus, the capacitor in COMPTON et al. is a fixed capacitor.

To summarize, a capacitor formed by first polysilicon layer 53, tunnel oxide layer 52, and N+ diffusion layer 51 is a fixed capacitor with a capacitance of 3 $fF/\mu m^2$. In this structure, since the N+ diffusion layer has a high impurity concentration, a depletion layer is not formed even if the voltage varies. Therefore, the capacitance is essentially constant, and the artisan would see that this device is a MOS capacitor and not a MOS varactor.

Further, the capacitor comprising N+ diffusion layer 51 and p-substrate 50 has an insignificant capacitance of 0.08 $fF/\mu m^2$, which is not a MOS varactor, as will be appreciated by one of skill in the art.

The difference in structure is caused by the different object of COMPTON et al., which is to increase a capacitance per unit area. By contrast, an object of the invention in claim 23

is to increase a variable amount of a capacitance.

Thus, COMPTON et al. do not disclose the claimed MOS varactor with a thinner insulating film than that of the MOS transistors, and thus the proposed combination does not disclose all the claim limitations. Accordingly, the claims avoid the rejection under §103.

Claim 36

Claim 36 is allowable for the same reasons as given above for claim 23.

In view of this, it is believed that the rejection of record cannot be sustained and that the same must be reversed and such is respectfully requested.

The claims involved in the appeal are set forth in the Claims Appendix.

There are no copies of evidence in the Evidence Appendix.

There are no copies of decisions in the Related Proceedings Appendix.

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If necessary, the Commissioner is hereby authorized in this, concurrent, and future submissions, to charge any underpayment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON

By _/Thomas W. Perkins/_____
Thomas W. Perkins
Attorney for Appellants
Registration No. 33,027
209 Madison Street, Suite 500
Alexandria, VA 22314
Telephone: 703/521-2297

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8. Claims Appendix

The claims on appeal:

1-22. (canceled)

23. A semiconductor integrated circuit device comprising:

a first conductivity type substrate;

MOS transistors disposed in said substrate and including first insulating films; and

an MOS type varactor element disposed in said substrate and including a second insulating film, a conductive electrode and a second conductivity type well,

wherein said second insulating film, said conductive electrode and said second conductivity type well form a variable capacitor,

wherein said first insulating films have a plurality of different thicknesses,

wherein a thickness of said second insulating film is thinner than that of the thinnest insulating film among said first insulating films of said MOS transistors, and

wherein first and second diffusion layers are provided at both sides of said conductive electrode, and said first and second diffusion layers are connected to a common terminal through first and second wiring line respectively.

24. The semiconductor integrated circuit device according

to claim 23, wherein a variable capacitance is formed between said conductive electrode and said second conductivity type well, and said variable capacitance is response to a voltage between said conductive electrode and said second conductivity type well.

25. The semiconductor integrated circuit device according to claim 23, wherein maximum gate voltage applied to said MOS type varactor element is lower than a minimum gate voltage applied to said MOS transistors.

26. The semiconductor integrated circuit device according to claim 23, wherein said MOS transistors include an N-channel MOS transistor and P-channel MOS transistor.

27. The semiconductor integrated circuit device according to claim 23, wherein said first and second diffusion layers are second conductivity type diffusion layers.

28. The semiconductor integrated circuit device according to claim 27, wherein said common terminal supplies with a potential of said second conductivity type well through said first and second diffusion layers.

29. The semiconductor integrated circuit device according to claim 23, wherein said first and second diffusion layers are first conductivity type diffusion layers.

30. The semiconductor integrated circuit device according

to claim 29, wherein said MOS type varactor element further comprises a third diffusion layer disposed in said second conductivity type well, said third diffusion layer is connected to a terminal different from said common terminal through a third wiring line.

31. The semiconductor integrated circuit device according to claim 30, wherein said third diffusion layer is a second conductivity type diffusion layer.

32. The semiconductor integrated circuit device according to claim 31, wherein said terminal supplies with a potential of said second conductivity type well through said third diffusion layer.

33. The semiconductor integrated circuit device according to claim 32, wherein said common terminal supplies said first and second diffusion layers with a ground potential.

34. The semiconductor integrated circuit device according to claim 23, wherein a thickness of said second insulating film of said MOS type varactor element is about three quarters of a thickness of first insulating films of said MOS transistors.

35. The semiconductor integrated circuit device according to claim 34, wherein the thickness of said second insulating film of said MOS type varactor element is about 6 nm.

36. A semiconductor integrated circuit device comprising:

a first conductivity type substrate;

MOS transistors disposed in said substrate and including first insulating films; and

an MOS type varactor element disposed in said substrate and including a second insulating film, a conductive electrode and a second conductivity type well,

wherein said second insulating film, said conductive electrode and said second conductivity type well form a variable capacitor,

wherein said first insulating films all have a same thickness,

wherein a thickness of said second insulating film is thinner than the same thickness of said first insulating films of said MOS transistors, and

wherein first and second diffusion layers are provided at both sides of said conductive electrode, and said first and second diffusion layers are connected to a common terminal through first and second wiring lines respectively.

37. The semiconductor integrated circuit device according to claim 36, wherein a variable capacitance is formed between said conductive electrode and said second conductivity type well, and said variable capacitance is response to a voltage between said conductive electrode and said second conductivity

type well.

38. The semiconductor integrated circuit device according to claim 36, wherein maximum gate voltage applied to said MOS type varactor element is lower than a minimum gate voltage applied to said MOS transistors.

39. The semiconductor integrated circuit device according to claim 36, wherein said MOS transistors include an N-channel MOS transistor and P-channel MOS transistor.

40. The semiconductor integrated circuit device according to claim 36, wherein said first and second diffusion layers are second conductivity type diffusion layers.

41. The semiconductor integrated circuit device according to claim 40, wherein said common terminal supplies with a potential of said second conductivity type well through said first and second diffusion layers.

42. The semiconductor integrated circuit device according to claim 36, wherein said first and second diffusion layers are first conductivity type diffusion layers.

43. The semiconductor integrated circuit device according to claim 42, wherein said MOS type varactor element further comprises a third diffusion layer disposed in said second conductivity type well, said third diffusion layer is connected to a terminal different from said common terminal through a

third wiring line.

44. The semiconductor integrated circuit device according to claim 43, wherein said third diffusion layer is a second conductivity type diffusion layer.

45. The semiconductor integrated circuit device according to claim 44, wherein said terminal supplies with a potential of said second conductivity type well through said third diffusion layer.

46. The semiconductor integrated circuit device according to claim 45, wherein said common terminal supplies said first and second diffusion layers with a ground potential.

47. The semiconductor integrated circuit device according to claim 36, wherein a thickness of said second insulating film of said MOS type varactor element is about three quarters of a thickness of first insulating films of said MOS transistors.

48. The semiconductor integrated circuit device according to claim 47, wherein the thickness of said second insulating film of said MOS type varactor element is about 6 nm and the thickness of first insulating films of said MOS transistors is about 8 nm.

49. The semiconductor integrated circuit device according to claim 23, wherein said MOS type varactor element has only one insulating film as a capacitor insulating film, the only one

insulating film being said second insulating film.

50. The semiconductor integrated circuit device according to claim 36, wherein said MOS type varactor element has only one insulating film as a capacitor insulating film, the only one insulating film being said second insulating film.

9. Evidence Appendix

None.

10. Related Proceedings Appendix

None.